

**Amendments to the Claims:**

Claims 26, and 28-30 have been canceled and claims 24 and 31 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Applicant respectfully requests that Please entry of the claims as amended herein.

**Listing of Claims:**

Claims 1-23. (Canceled)

24. (Currently Amended) An electronic device, comprising:  
a semiconductor substrate;  
an electrically conductive layer disposed on at least one side of the semiconductor substrate,  
comprising;  
a voltage reference plane substantially covering the at least one side of the semiconductor  
substrate and configured for operable coupling to a voltage reference signal;  
a plurality of signal trace slots disposed in the voltage reference plane; and  
a plurality of signal traces disposed in the plurality of signal trace slots;  
wherein the plurality of signal traces are electrically isolated from the voltage reference  
plane by a gap in the electrically conductive layer with a gap distance sufficient to  
avoid an electrical short between the plurality of signal traces and the voltage  
reference plane; and  
wherein the voltage reference plane provides a continuous electrical connection around  
each of the plurality of signal trace slots such that at least a portion of the voltage  
reference plane is disposed between any two of the plurality of signal traces to  
reduce cross talk between signals carried by the any two of the plurality of signal  
traces; and  
a plurality of solder balls disposed on the at least one side of the semiconductor substrate,  
wherein at least one of the plurality of solder balls is operably coupled to at least one of

the plurality of signal traces and at least one of the plurality of solder balls is operably coupled to the voltage reference ~~signal~~ signal;  
wherein at least one of the plurality of signal traces includes at least one direction change in the length thereof over the semiconductor substrate.

25. (Previously Presented) The electronic device of claim 24, further comprising a passivation layer disposed on the electrically conductive layer.

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Currently Amended) An electronic system, comprising:  
a processor;  
a memory device;  
at least one input device;  
at least one output device; and  
at least one data storage device;  
wherein at least one of the processor, the memory device, the at least one input device, the at least one output device and the at least one data storage device includes an electronic device comprising:  
a semiconductor substrate; and

an electrically conductive layer disposed on at least one side of the semiconductor substrate, comprising;

a voltage reference plane substantially covering the at least one side of the semiconductor substrate and configured for operable coupling to a voltage reference signal;

a plurality of signal trace slots disposed in the voltage reference plane; and

a plurality of signal traces disposed in the plurality of signal trace slots;

wherein the plurality of signal traces are electrically isolated from the voltage reference plane by a gap in the electrically conductive layer with a gap distance sufficient to avoid an electrical short between the plurality of signal traces and the voltage reference plane; and

wherein the voltage reference plane provides a continuous electrical connection around each of the plurality of signal trace slots such that at least a portion of the voltage reference plane is disposed between any two of the plurality of signal traces to reduce cross talk between signals carried by the any two of the plurality of signal traces; and

a plurality of solder balls disposed on the at least one side of the semiconductor substrate, wherein at least one of the plurality of solder balls is operably coupled to at least one of the plurality of signal traces and at least one of the plurality of solder balls is operably coupled to the voltage reference ~~signal~~ signal;

wherein at least one of the plurality of signal traces includes at least one direction change in the length thereof over the semiconductor substrate.